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FORM PTO-1390 (REV 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. 107400-00043
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		DATE: October 30, 2001
		U.S. APPLN. NO. (IF KNOWN, SEE 37 C.F.R. 1.5) Not Yet Assigned 09/926425

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/02867	28 April 2000	30 April 1999 & 14 May 1999

TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH BIPOLAR TRANSISTOR

APPLICANT(S) FOR DO/EO/US: Kazuhisa SAKAMOTO

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
(THE BASIC FILING FEE IS ATTACHED)

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures [35 U.S.C. 371(f)] at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper demand for International Preliminary Amendment was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed [35 U.S.C. 371(c)(2)]
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

6. ☒ A translation of the International Application into English [35 U.S.C. 371(c)(2)].

7. ☒ Amendments to the claims of the International Application under PCT Article 19 [35 U.S.C. 371(c)(3)]
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 [35 U.S.C. 371(c)(3)].

9. ☒ An oath or declaration of the inventor(s) [35 U.S.C. 371(c)(4)].

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 [35 U.S.C. 371(c)(5)].

Items 11 - 16 below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.
☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information: ☒ Front page of the published international application; Amended under 34 article claims; PCT/ISA/210
Drawings (13 sheets)

U.S. APPLN. NO. (IF KNOWN SEE 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY DOCKET NO.
Not Yet Assigned 09/926425	PCT/JP00/02867	107400-00043
		DATE: October 30, 2001

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee [37 C.F.R. 1.492(a)(1)-(5)]:		
Search Report has been prepared by the EPO or JPO.....$890.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482).....$710.00		
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO [37 C.F.R. 1.445(a)(2)].....$740.00		
Neither international preliminary examination fee (37 C.F.R. 1.482) or international search fee [37 C.F.R. 1.445(a)(2)] paid to USPTO.....$1,040.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4).....$ 100.00		

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date [37 C.F.R. 1.492(e)].				$ 0.00	
Claims	Number Filed	Number Extra	Rate		
Total Claims	10 - 20 =	0	X $ 18.00	$ 0.00	
Independent Claims	6 - 3 =	3	X $ 84.00	$ 252.00	
Multiple dependent claim(s) (if applicable)			+ $280.00	$ 280.00	
TOTAL OF ABOVE CALCULATIONS =				$ .00	
Reduction by one-half for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28).				$ 0.00	
SUBTOTAL =				$ 1,422.00	
Processing fee of $130.00 for furnishing the English translation later the ☐ 20 ☐ 30 months from the earliest claimed priority date [37 C.F.R. 1.492(f)]. +				$ 0.00	
TOTAL NATIONAL FEE =				$ 1,422.00	
Fee for recording the enclosed assignment [37 C.F.R. 1.21(h)]. The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$ 1,462.00	
				Amount to be refunded	$
				Charged	$

a. ☐ A check in the amount of $ to cover the above fees is enclosed.
b. ☒ Please charge my Deposit Account No. 01-2300 in the amount of $1,462.00 to cover the above fee. A duplicate copy of this sheet is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2300.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive [37 C.F.R. 1.137(a) or (b)] must be filed and granted to restore the application to pending status.

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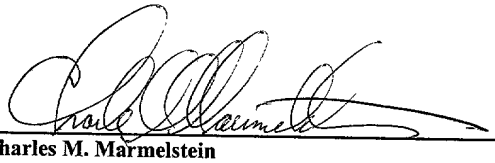

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Amendment

(based on Japanese Law Article 11)

Kozo Oikawa Commissioner of the Patent Office

1. Indication of International Application PCT/JP00/02867

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4. Object of Amendment Claims

5. Contents of Amendment

(1) Claims 1, 2, 3, 4, 5, 9 and 11 are amended as shown in the annexed substitution sheet.

(2) Claims 6, 7, 8 and 10 are deleted.

6. List of Annexation

(1) Claims 17 to 18/2 pages.

What is claimed is:

1. (Amended) A semiconductor device with a bipolar transistor comprising:

a first conductivity type semiconductor layer serving as a collector region;

a base region constituted of a second conductivity type region provided in said first conductivity type semiconductor layer;

an emitter region constituted of a first conductivity region provided in said base region; and

a base contact section provided oppositely from said emitter region in said base region, electrically connected to a base electrode,

wherein said base contact section is constructed of a repeating structure in a plan view, in which a high impurity concentration region of the second conductivity type and a region of the first conductivity type are arranged in an alternate manner, and

wherein said emitter region comprises a plurality of stripe regions and each of said stripe regions is formed so that said base region is exposed at the central portion of each of said stripe regions to be segmented into a plurality along a direction of the stripe, and an emitter electrode is formed so as to be connected to said stripe regions and to cover exposed portions of said base region via an insulating film on said stripe regions and said exposed portions of said base region.

2. (Amended) A semiconductor device with a bipolar transistor comprising:

a first conductivity type semiconductor layer serving as a collector region;

a base region constituted of a second conductivity type region provided in said first conductivity type semiconductor layer;

an emitter region constituted of a first conductivity region provided in said base region; and

a base contact section provided oppositely from said emitter region in said base region, electrically connected to a base electrode,

wherein said base contact section is constructed of a repeating structure in a plan view, in which a high impurity concentration region of the second conductivity type and a region of the second conductivity type constituting said base region are arranged in an alternate manner, and

wherein said emitter region comprises a plurality of stripe regions and each of said stripe regions is formed so that said base region is exposed at the central portion of each of said stripe regions to be segmented into a plurality along a direction of the stripe, and an emitter electrode is formed so as to be connected to said stripe regions, and to cover exposed portions of said base region via an insulating film on said stripe regions and said exposed portions of said base region.

3. (Amended) A semiconductor device with a bipolar transistor comprising:

a first conductivity type semiconductor layer serving as a collector region;

a base region constituted of a second conductivity type region provided in said first conductivity type semiconductor layer;

an emitter region constituted of a first conductivity region provided in said base region; and

a base contact section provided oppositely from said emitter region in said base region, electrically connected to a base electrode,

wherein said base contact section is constructed of a repeating structure in a plan view, in which a high impurity concentration region of the second conductivity type and a region of the first conductivity type are arranged in an alternate manner, and

wherein said emitter region comprises a plurality of stripe regions and each of said stripe regions is formed so that said base region is exposed at the central portion of each of said stripe regions to be segmented along a direction of the stripe into two segmented stripe regions, and an emitter electrode is formed so as to be connected to said stripe regions and to cover exposed portions of said base region via an insulating film on said segmented stripe regions and said base region therebetween.

4. (Amended) A semiconductor device with a bipolar

transistor comprising:

a first conductivity type semiconductor layer serving as a collector region;

a base region constituted of a second conductivity type region provided in said first conductivity type semiconductor layer;

an emitter region constituted of a first conductivity region provided in said base region; and

a base contact section provided oppositely from said emitter region in said base region, electrically connected to a base electrode,

wherein said base contact section is constructed of a repeating structure in a plan view, in which a high impurity concentration region of the second conductivity type and a region of the second conductivity type constituting said base region are arranged in an alternate manner, and

wherein said emitter region comprises a plurality of stripe regions and each of said stripe regions is formed so that said base region is exposed at the central portion of each of said stripe regions to be segmented along a direction of the stripe into two segmented stripe regions, and an emitter electrode is formed so as to be connected to said stripe regions and to cover exposed portions of said base region via an insulating film on said segmented stripe regions and said base region therebetween.

5. (Amended) A semiconductor device according to

claim 1, 2, 3 or 4, wherein an emitter electrode connected to said emitter region and a base electrode connected to said base contact section are formed in respective comb structures in which teeth of said emitter electrode and said base electrode are engaged with each other being alternately arranged.

6. (Deleted)

7. (Deleted)

8. (Deleted)

9. (Amended) A semiconductor device with a bipolar transistor comprising:

a first conductivity type semiconductor layer serving as a collector region;

a base region constituted of a second conductivity type region provided in said first conductivity type semiconductor layer;

an emitter region constituted of a first conductivity region provided in said base region; and

a base contact section provided oppositely from said emitter region in said base region, electrically connected to a base electrode,

wherein said emitter region comprises a plurality of stripe regions and each of said stripe regions is formed so that said base region is exposed at the central portion of each of said stripe regions to be segmented into a plurality along a direction of the stripe, and an emitter electrode is formed so as to be connected to said stripe

regions and to cover exposed portions of said base region.

10. (Deleted)

11. (Amended) A semiconductor device with a bipolar transistor comprising:

a first conductivity type semiconductor layer serving as a collector region;

a base region constituted of a second conductivity type region provided in said first conductivity type semiconductor layer;

an emitter region constituted of a first conductivity region provided in said base region; and

a base contact section provided oppositely from said emitter region in said base region, electrically connected to a base electrode,

wherein said emitter region comprises a plurality of stripe regions and each of said stripe regions is formed so that said base region is exposed at the central portion of each of said stripe regions to be segmented along a direction of the stripe into two segmented stripe regions, and an emitter electrode is formed so as to be connected to said stripe regions and to cover exposed portions of said base region via an insulating film on said segmented stripe regions and said base region therebetween.

13/prts

SEMICONDUCTOR DEVICE WITH BIPOLAR TRANSISTOR

FIELD OF THE INVENTION

[0001] The present invention relates to a semiconductor device with a bipolar transistor having a high switching speed and an improved withstand voltage. More particularly, the invention relates to a semiconductor device with a bipolar transistor having a multi-emitter or a multi-base structure that can operate with a large current, a high withstand voltage, a high speed switching and an increased safe operation area (SOA).

BACKGROUND ART

[0002] A fundamental structure of a conventional bipolar transistor is shown in FIG. 17. That is, in the bipolar transistor, a P-type base region 12 is formed in a surface layer of an N-type semiconductor substrate 1 and an N-type emitter region 13 is formed in the P-type base region 12. A base electrode 15 and an emitter electrode 16 are in contact with the base region 12 and the emitter region 13, respectively. A collector electrode is to be formed at the back surface side of the N-type semiconductor substrate 1 through an N^+-type region 14. A numerical mark 17 indicates an insulation film.

[0003] In order to increase a current amplification factor, an impurity concentration in the base region 12 is necessary to be low. If the impurity concentration is

excessively lowered, however, a contact between the base region 12 and the base electrode 15 works as a Schottky junction, which makes it impossible to obtain transistor characteristics. Therefore, a P^+-region 18 for formation of an ohmic junction is formed at a contact region of the base region 12, with which the base electrode 15 is in contact.

[0004] Further, in a transistor which requires a large current in operation, an area and perimetric length of an emitter are increased so as to reduce a current density since a magnitude of a collector current depends mainly on the area and perimetric length of an emitter. Therefore, as shown in pattern examples of an emitter region 13 of FIGS. 17 to 20, a bipolar transistor with a multi-emitter structure or a multi-base structure has been considered.

[0005] FIG. 18 shows a structure of a bipolar transistor of a mesh emitter (multi-emitter) type. In this transistor, insular emitter regions 13 are arranged in a grid pattern, being embedded in a base region 12 formed in the surface layer of a semiconductor substrate 15. Further, an emitter electrode (not shown) is in common contact with the insular emitter regions 13.

[0006] FIG. 19 shows a structure of a bipolar transistor of a ring emitter (mesh base; multi-base) type. In this transistor, an broadly extended emitter region 13 are formed in a base region 12 formed in the surface layer of a semiconductor substrate 1. In such a large area emitter region 13, the base region 12 are exposed as islands

arranged in a grid pattern. Further, contacts to connect a base electrode (not shown) and the base region 12 are effected at the exposed portions.

[0007] FIG. 20 shows a structure of a bipolar transistor of a stripe emitter type. In this structure, a plurality of long, narrow emitter regions 13 are arranged in almost parallel, being embedded in a base region 12 extended over the surface layer of a semiconductor substrate 1.

[0008] As described above, when, in these structures, an impurity concentration is low in a base region but high in a contact region of an electrode thereof, electrons, which are minority carriers, are blocked by a P/P^+ junction between the base region 12 and a P^+-type region 18 and in a switching operation, electrons are accumulated in the base region 12. This accumulation of electrons comes with a problem, since a switching loss becomes large, thereby not only preventing a high speed switching, (especially extending an off time,) but causing increase in power consumption.

[0009] Further, in transistors of a mesh emitter type shown in FIG. 18 and a ring emitter type shown in FIG. 19, safe operation areas of both types are comparatively narrow and withstand voltages are not necessarily sufficient. For the reasons, there arises a problem, since a sufficient current cannot be supplied to a load.

[0010] Furthermore, with a stripe emitter type of FIG. 20 being adopted, a withstand voltage is improved, but a case

arises where a load driving ability is not sufficient. Among other points, a switching time of a transistor of this stripe emitter type is good compared with those of a mesh emitter type and a ring emitter type, but there arises a case where a further higher speed switching operation is required.

[0011] It is an object of the invention to provide a semiconductor device with a bipolar transistor enabling not only a high speed switching operation but reduction in power consumption.

[0012] It is another object of the invention to provide a semiconductor device with a bipolar transistor enabling a safe operation area to be wider.

[0013] It is still another object of the invention to provide a semiconductor device with a bipolar transistor enabling a reduction in voltage in an on state to be realized.

DISCLOSURE OF THE INVENTION

[0014] A semiconductor device with a bipolar transistor according to the invention comprises: a first conductivity type semiconductor layer serving as a collector region; a base region constituted of a second conductivity type region provided in the first conductivity type semiconductor layer; an emitter region constituted of a first conductivity region provided in the base region; and a base contact section provided oppositely from the emitter region in the base

region, electrically connected to a base electrode, wherein the base contact section is constructed of a repeating structure in a plan view, in which a high impurity concentration region of the second conductivity type and a region of the first conductivity type are arranged in an alternate manner starting with the high impurity concentration region from a side of the emitter region.

[0015] For example, if the base region is a P-type region, the base contact section is constructed of a structure in which P^+-type region and N^+-type region are alternately arranged with the outermost side is of P^+-type. With such a structure, minority carriers in the base region, for example electrons in a case of a P-type base region, fall in N^+-type region, thereby enabling accumulation of minority carriers in the base region to be prevented from occurring. With prevention of the accumulation of minority carriers in the base region, a switching operation can not only be of a high speed, but reduce a switching loss, with the result that reduction in power consumption can be realized.

[0016] Another embodiment of a bipolar transistor according to the invention comprises: a first conductivity type semiconductor layer serving as a collector region; a base region constituted of a second conductivity type region provided in the first conductivity type semiconductor layer; an emitter region constituted of a first conductivity region provided in the base region; and a base contact section provided oppositely from the emitter region in the base

region, electrically connected to a base electrode, wherein the base contact section is constructed of repeating structure in a plan view, in which a high impurity concentration region of the second conductivity type and a low impurity concentration region of the second conductivity type constituting the base region are arranged in an alternate manner starting with the high impurity concentration region from a side of the emitter region.

[0017] In this structure as well, since the low impurity concentration region contacts the base electrode to form Schottky junctions at the interfaces, minority carriers coming to the base electrode side due to an off state of operation are not accumulated in the base contact section but quickly released out through the Schottky junctions. As a result, similar to the above described structure, not only can an switching operation be of a high speed, but a switching loss decrease and reduction in power consumption can be achieved.

[0018] The emitter region comprises a plurality of stripes and the base contact section comprises a plurality of contact sections formed along each of the plurality of stripes in the base region between the plurality of stripes, or the base region comprises a plurality of regions exposed in a matrix pattern in the emitter region and the base contact section comprises a plurality of contact sections formed at each of a plurality of regions of the base region exposed in the matrix (island) pattern, thereby enabling

realization of a bipolar transistor capable of a large current operation.

[0019] If an emitter electrode connected to the emitter region and a base electrode connected to the base contact section are formed in respective comb structures in which teeth of the emitter electrode and the base electrode are engaged with each other being alternately arranged, the base and emitter electrodes can be connected to the base region and the emitter region, respectively, located in the vicinity thereof at a low level of resistance loss.

[0020] The emitter region comprises a plurality of stripe regions and the stripe regions are formed so as to expose the base region at respective central portions of the stripe regions and an emitter electrode is formed, being connected to the emitter regions, so as to cover the exposed portions of the base region, and thereby, since no electrode is formed in the exposed portions of the base region at the central portion of the stripe regions, there arises no necessity of a space to form base electrode, which enables to increase a contact area between the emitter region and the base region to about twice, and the safe operation area is sufficiently enlarged. With this structure being adopted together with the base contact section, the switching speed can be high, and the safety operation area can also enlarged sufficiently, but furthermore, a safety operation area can be wider with this structure adopted, independently of a structure of the base contact section.

[0021] The base region exposed at the central portion of each of the stripe regions may be segmented into a plurality along a direction of the stripe, or the base region exposed at the central portion of each of the stripe regions may be provided such that each of the stripe regions is segmented along a direction of the stripe and the emitter electrode may be formed over the two segmented stripe regions and the base region exposed therebetween.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] FIG. 1 is a sectional view showing a fundamental structure of a bipolar transistor relating to an embodiment of a semiconductor device according to the present invention;

[0023] FIG. 2 is an enlarged, sectional view showing a structure in the vicinity of a base contact section of FIG. 1;

[0024] FIG. 3 is an electrical circuit diagram showing a configuration of a switching circuit using a bipolar transistor;

[0025] FIGS. 4(a) to 4(c) are graphs of waveforms for description of operating characteristics of a bipolar transistor;

[0026] FIG. 5 is a plan view showing a concrete structure of a bipolar transistor according to the present invention;

[0027] FIG. 6 is an enlarged, plan view showing a structure of a base contact section of FIG. 5;

[0028] FIG. 7 is a plan view showing electrodes arrangement of the example shown in FIG. 5;

[0029] FIG. 8 is a plan view showing another concrete structure of a bipolar transistor;

[0030] FIG. 9 is an enlarged, plan view showing a structure of a base contact section of FIG. 8;

[0031] FIG. 10 is a plan view showing electrodes arrangement of the example shown in FIG. 8;

[0032] FIG. 11 is a sectional view showing another embodiment of a base contact section of a semiconductor device according to the present invention;

[0033] FIG. 12 is a perspective view showing still another embodiment of a semiconductor device according to the present invention;

[0034] FIG. 13 is a view showing a plane arrangement of FIG. 12;

[0035] FIG. 14 is an enlarged, plan view showing a structure of a base contact section of FIG. 13;

[0036] FIG. 15 is a graph showing switching characteristics of the example of FIG. 12;

[0037] FIG. 16 is a plan view showing a modification of the embodiment of FIG. 12;

[0038] FIG. 17 is a sectional view showing a fundamental structure of a conventional bipolar transistor;

[0039] FIG. 18 is a simplified, perspective view for description of a bipolar transistor of a mesh emitter (multi-emitter) structure;

[0040] FIG. 19 is a simplified, perspective view for description of a bipolar transistor of a ring emitter (multi-base) structure; and

[0041] FIG. 20 is a simplified perspective view for description of a bipolar transistor of a stripe emitter structure.

BEST MODE FOR CARRYING OUT THE INVENTION

[0042] FIG. 1 is a sectional view showing a fundamental structure of a bipolar transistor relating to an embodiment of the invention. A P-type base region 22 is formed at the surface of an N-type semiconductor layer 21 and an N-type emitter region 23 is formed in the P-type base region 22. With such regions in place, an NPN structure is formed and the N-type semiconductor layer 21 and an N^+-type semiconductor substrate 21a constitute a collector region.

[0043] At the surface of the base region 22, a base contact section in which a P^+-type region and an N^+-type region are alternately formed (such a base contact section hereinafter will be referred to as a universal contact section 25) is provided at a position spaced from the emitter region 23 and a base electrode 26 is in contact with the universal contact section 25. Further, an emitter electrode 26 is in contact with the emitter region 23. A collector electrode 30 is formed at the back surface side of the semiconductor substrate 21a. A numerical mark 29 indicates an insulation film.

[0044] FIG. 2 is an enlarged, sectional view showing a structure in the vicinity of the universal contact section 25. In the example shown in FIG. 2, the universal contact section 25 is constructed of a plurality of P^+-type regions 251 of a small width and a plurality of N^+-type regions 252 of a small width arranged alternately while being in contact with the base electrode 26. That is, the P-type region 251 and the N-type region 252 are alternately arranged along a cross direction to a direction in which the electrical charges move between the base region 22 and the base electrode 26.

[0045] With such a structure, holes in the base region 22, which are majority carriers, can move through the P^+-type region 251 while electrons, which are minority carriers, can fall in the N^+-type region 252. Therefore, accumulation of electrons in the base region 22 is suppressed, thereby enabling a switching with a high speed and less of a loss.

[0046] FIG. 3 is a electrical circuit diagram showing a configuration of a switching circuit using a bipolar transistor (Tr) and FIGS. 4(a) to 4(c) are graphs showing switching characteristics of a bipolar transistor (Tr), wherein FIG. 4(a) shows a base current I_B, FIG. 4(b) shows a collector current I_C and FIG. 4(c) shows a collector-emitter voltage V_{CE}. In FIGS. 4(b) and 4(c), characteristics when the bipolar transistor of FIG. 1 is applied to the transistor (Tr) are shown with a solid line while characteristics when a conventional bipolar transistor shown

in 16 is applied to the transistor (Tr) are shown with a double dot & dash line.

[0047] As is clear from FIGS. 4(a) to 4(c), it is understood that a turn off time T_{off} (= T_{stg} + T_f) which is a sum of a storage time (T_{stg}) and a decay time (T_f) when the transistor (Tr) is turned off is conspicuously improved if a bipolar transistor having a universal contact of this embodiment is employed.

[0048] The time T_{off} required to reduce accumulation of carriers in the base region 22 to nothing can be shorter to about one half to about one-thirds of in a case of a conventional structure by adopting the structure of this embodiment. A power loss of the transistor (Tr) in an off state can be expressed with areas of respective regions SI (in the case of the structure of this embodiment) and SP (in the case of the conventional structure) in FIG. 4(c) and to be more concrete, the loss can be expressed by the following formula (1):

$$\frac{1}{2}\mathrm{Ic}\cdot V_{CE}(\mathrm{sat})\cdot(\mathrm{Tstg}/\mathrm{T})+\frac{1}{6}\mathrm{Ic}\cdot\mathrm{Vcc}\cdot\mathrm{Tf} \qquad (1)$$

where T represents a cycle time.

[0049] Therefore, when a bipolar transistor of this embodiment which can shorten the time T_{off} by a great margin is employed, power consumption can be also reduced tremendously. In addition, with this structure applied, it was confirmed that the safe operation area can be improved to the same level as that of the stripe emitter type.

[0050] FIG. 5 is a plan view showing a concrete structure of a bipolar transistor of a stripe emitter type relating to this embodiment. In the base region 22, there are formed emitter (stripe) regions 23 of a pattern constituted of a plurality of strips repeating in a direction, leftward and rightward, on FIG. 5. A universal contact section 25 is formed in a belt form such that the universal contact section winds around each of edges of the emitter regions 23 and penetrate into between adjacent emitter (stripe) regions 23.

[0051] As shown in FIG. 6 in an enlarged manner, the belt-like universal contact section 25 is formed along its length direction, and includes belt-like P^+-type regions 251 and N^+-type belt-like regions 252 arranged alternately in its width direction.

[0052] An insulation film (not shown) is formed so as to cover the emitter regions 23 and a universal contact section 25 and, in the insulation film, a plurality of contact holes 35 are formed through which contact holes the emitter regions 23 are exposed and a plurality of contact holes (not shown) are formed through which contact holes the universal contact section 25 is exposed. As shown in FIG. 7, the emitter electrode 27 is formed so as to be commonly connected to the plurality of contact holes 35 and the base electrode 26 is formed so as to be connected to the plurality of contact holes through which the universal contact section 25 is exposed. The base electrode 26 and

the emitter electrode 27 may be formed in patterns of combs, as shown in FIG. 7, which teeth are engaged with each other in a alternate manner.

[0053] FIG. 8 is a plan view showing another concrete structure of a bipolar transistor relating to the above described embodiment. This example is of a multi-base structure and exposed sections 22E of the base region 22 are arranged in a matrix pattern of dots and in other regions than the base region 22, the emitter region 23 is exposed at a surface of the semiconductor substrate. The universal contact sections 25 are formed in the exposed sections 22E.

[0054] That is, as shown in FIG. 9 in enlarged manner, the P^+-type regions 251 and the N^+-type regions 252 formed in concentric circles are alternately arranged in a radial direction to form a universal contact section 25.

[0055] In this structure as well, as shown in FIG. 10, the base electrode 26 and the emitter electrode 27 can be in a pattern of combs whose teeth are engaged with each other in a alternate manner. The base electrode 26 is in contact with the universal contact sections 25 through contact holes (not shown) and the emitter electrode 27 is in contact with the emitter region 23 through contact holes 35 (see FIG. 8) formed in place.

[0056] FIG. 11 is an enlarged, sectional view showing a universal contact section of a bipolar transistor relating to another embodiment of the present invention. In FIG. 11, constituents corresponding to those in FIG. 2 are indicated

by the same marks as those used in the case of FIG. 2. In this embodiment, a universal contact section 25 is formed so as to be included in a P-type base region 22 and constituted of a plurality of P^+-type regions 251 arranged in a manner such that any adjacent two are spaced from each other along a cross direction to a direction in which the electrical charges move. In a space between adjacent P^+-type regions 251, a Schottky junction is formed between the base electrode 26 and the P-type base region 22 and further, the P^+-type regions 251 and the Schottky junctions are alternately arranged to form the Schottky universal contact.

[0057] In this structure, minority carriers accumulated in the base region 22 can be quickly released out through the Schottky junctions. With the release of minority carriers, similar to the above described first embodiment, accumulation of minority carriers in the base region 22 can be suppressed, thereby enabling not only a high speed switching operation but low power consumption driving.

[0058] While the two embodiments of the present invention have been described, the invention can be also carried out in other embodiments. For example, in the above described embodiments, an NPN transistor has been taken as an example, the present invention can be applied to a PNP transistor as well. In the case of PNP transistor, there is only require to be provided a universal contact section of a configuration in which N^+-type regions and P^+-regions are alternately arranged in an N-type base region or a universal

contact section with Schottky junctions of a configuration in which a plurality of N^+-type regions are arranged in a spaced manner. Furthermore, electrode materials such as titanium (Ti), in addition to aluminum (Al), can be used in the Schottky junction sections.

[0059] In addition, while in the above described embodiments, a semiconductor device with a single bipolar transistor has been taken up, the present invention can be applied to a semiconductor device with a plurality of bipolar transistors and a semiconductor device with functional elements other than a bipolar transistor together with the bipolar transistor on the same semiconductor substrate.

[0060] FIG. 12 is an enlarged, perspective view together with a sectional view showing a structure of part of a transistor of an example in which a safe operation area is further widened. A P-type base region 22 is formed at a surface of an N-type semiconductor layer 21 and N-type emitter regions 23 are formed on the surface side of the P-type base region 22 in the stripe form. With this structure, an NPN structure is formed and an N-type semiconductor layer 21 and a semiconductor substrate 21a constitute a collector region 21.

[0061] As shown in a plan view of FIG. 13, the emitter regions 23 are each formed in a closed ring pattern extending linearly in one direction. The emitter regions 23 of a linear ring pattern are formed in plural number while

being exposed in a stripe pattern on a semiconductor layer 21. Base contact sections 25 of a linear ring pattern are provided so as to enclose the respective emitter regions 23 of a linear ring pattern at a constant distance between an emitter region 23 and the innermost base contact section 25.

[0062] As shown in FIG. 14 in an enlarged manner, the emitter regions 23 are arranged over almost the entire width of the base region 22, and each comprise a pair of straight portions 23A and 23B parallel to each other and connection sections 23C of a semicircular shape, connecting between both ends of one side or the other side of the straight portions 23A and 23B of a pair with an opening 23D inside of the emitter region 23 in which the base region 25 comes.

[0063] As shown in FIG. 12, a base electrode 26 is in contact with base contact sections 25. Further, a contact region 35 of a linear ring pattern with a narrower width than that of the emitter region 23 is provided at the surface of the emitter region 23 of a linear ring pattern and at the contact region 35, an emitter electrode 27 is in contact with the emitter region 23. A collector electrode 30 is provided at the rear (back) surface side of the semiconductor substrate 21a. A numerical mark 29 is an insulation film.

[0064] A base contact section 25 has a universal contact in which P^+-type regions 251 with a small width and N^+-type regions 252 with a small width are alternately arranged while being in contact with a base electrode 26. That is,

the P^+-type regions 251 and the N^+-type regions 252 are alternately arranged along a cross direction to a direction in which electrical charges move between the base region 22 and the base electrode 26. In a plan view, as shown in FIG. 14 in an enlarged manner, the P^+-type regions 251 and the N^+-type regions 252 are of a belt pattern extending along a length direction of the base contact section 25 of a ring belt pattern.

[0065] With this structure, as described above, holes, which are majority carriers, in the base region 22 can pass through the P^+-type regions 251 while electrons, which are minority carriers, in the base region 22, can fall into the N^+-type regions 252. Therefore, accumulation in the base region 22 is suppressed, thereby enabling switching with a high speed and less of a loss.

[0066] A plurality of contact holes 41 (see FIG. 12) through which the contact regions 35 of a ring pattern are exposed and a plurality of contact holes 42 through which the base contact sections 25 are exposed are formed in an insulation film 29 formed so as to cover the emitter regions 23 and the base contact sections 25. Similar to FIG. 7, which is described above, the emitter electrode 27 is formed so as to be commonly communicated with the contact holes 41 for a plurality of emitter regions 23 while the base electrode 26 is formed so as to be commonly communicated with the contact holes 42 through which a plurality of base contact sections 25 are exposed. The base electrode 26 and

the emitter electrode 27 may be formed in comb patterns whose teeth are engaged with each other as shown in FIG. 7.

[0067] When the switching circuit as shown in FIG. 3 is configured using this transistor, a collector-emitter voltage VCE characteristic similar to FIG. 4(c) is shown in FIG. 15, so that similar effects of the above described are attained on switching time and power loss in an off state and furthermore a sufficient current can be made to flow to a load, and thereby, it is understood that a safe operation area is wider and a withstand voltage can be increased.

[0068] Therefore, when a bipolar transistor of this embodiment in which a time T_{off} can be exceptionally shortened is employed, power consumption can be reduced to a great degree Besides, in the structure of this embodiment adopting an emitter region 23 of a linear ring pattern, a collector-emitter voltage V_{CE} (sat) in an on state can be reduced to 50 % of that of a conventional structure, whereby a power loss can be reduced as well.

[0069] In the structure of this embodiment, the emitter regions are arranged as stripes in parallel each of a linear ring pattern. Therefore, as is apparent from comparison between FIGS. 12 and 20, an area of emitter-base junctions is about twice as large as that in a conventional structure. That is, the emitter regions 23 of this embodiment can have a perimetric length of about twice that of a conventional structure in the neighborhood of the surface of semiconductor substrate where a current is apt to

concentrate because of a skin effect. With this increase in the perimetric length, a low current density at the base-emitter junction interface is realized when a current is made to flow, thereby enabling to suppress rise in temperature at the junction interface. With this suppression of temperature rise, a large current can be passed, which makes it possible to achieve a good withstand voltage and ensure a wider safe operation area.

[0070] Although this structure is likely to be similar to a stripe emitter structure with a narrower emitter width than that as shown in FIG. 20 for example, it is different from the stripe emitter structure in that a contact area between emitter regions and a base region can be increased in a narrow chip area, since in the case of FIG. 20, base electrodes are formed in contact with all base regions between the emitter regions and thereby, widths of the emitter electrodes and the base electrodes cannot be equal to or less than certain widths which are less than the maximums, while in this embodiment, no contact is formed in base regions provided within ring emitter regions and in addition to this, an emitter electrode is formed between emitter regions extending across a base region interposed therebetween.

[0071] From this viewpoint, it is concluded that when a structure is adopted in which an emitter electrode is formed between adjacent two emitter regions of a stripe pattern in a straddling manner, that is, a base region with no contact

is formed in a central portion of a conventional stripe emitter, even if the emitter regions are not of a linear ring pattern as in the above described example. With this structure as well, a contact area between the base region and the emitter region is doubled, thereby enabling a safe operation area to be increased to a great extent. To be concrete, it has been confirmed that in any of cases of a resistance load and an inductive load, a withstand voltage of about twice as large as that of a conventional structure can be realized.

[0072] In this example, an NPN transistor is taken for description, but the present invention can be applied to a PNP transistor as well. In the case of a PNP transistor, the following universal contact structures are only required to be formed in the base electrode contact section: a universal contact structure in which N^+-type regions and P^+-type regions are alternately arranged in an N-type base region, or a Schottky universal contact structure in which a plurality of N^+-type regions are arranged in a spaced manner. Further, the Schottky sections may be formed with titanium (Ti), in addition to aluminum (Al).

[0073] It is recommended that as a semiconductor substrate 21, a substrate of a resistivity as low as of the order of 7 $\Omega \cdot$ cm (corresponding to an impurity concentration of the order of about 1 x 10^{21} atoms/cm^3) doped with an impurity (for example, arsenic in a case of an N-type and boron in a case of a P-type) may be employed and thereby, a

collector-emitter voltage V_{CE} is further reduced.

[0074] In addition, while in the above described embodiment, description is made of an example in which emitter regions of a linear ring pattern and a universal contact structure are combined, the universal contact structure may be omitted when only reduction in a collector-emitter voltage VCE and improvement on a withstand voltage are important tasks but improvement on a switching time is not so much concerned.

[0075] Further, while in the above embodiment, an linear emitter region 23 is of a simple ring structure with one opening 23D, a modification of the linear ring structure may be adopted, as shown in FIG. 16, in which bridge sections 23E bridging the straight sections 23A and 23B are provided and the opening 23D is divided into plural openings.

[0076] Furthermore, while in the above embodiment, a semiconductor device having one bipolar transistor is taken as an example, the invention can be applied to a semiconductor device with a plurality of bipolar transistors and a semiconductor device with functional devices other than a bipolar transistor together with a bipolar transistor on the same semiconductor substrate.

INDUSTRIAL APPLICABILITY

[0077] According to the present invention a semiconductor device with a bipolar transistor is obtained, which has the high speed switching operation and the improved withstand

voltage. As a result, it is utilized in switching power supplies, DC-DC converters in the consumer electric equipment such as televisions, computers, telephones and the like, and so on.

What is claimed is:

1. A semiconductor device with a bipolar transistor comprising:

a first conductivity type semiconductor layer serving as a collector region;

a base region constituted of a second conductivity type region provided in said first conductivity type semiconductor layer;

an emitter region constituted of a first conductivity region provided in said base region; and

a base contact section provided oppositely from said emitter region in said base region, electrically connected to a base electrode,

wherein said base contact section is constructed of a repeating structure in a plan view, in which a high impurity concentration region of the second conductivity type and a region of the first conductivity type are arranged in an alternate manner from a side of said emitter region.

2. A semiconductor device with a bipolar transistor comprising:

a first conductivity type semiconductor layer serving as a collector region;

a base region constituted of a second conductivity type region provided in said first conductivity type semiconductor layer;

an emitter region constituted of a first conductivity region provided in said base region; and

a base contact section provided oppositely from said emitter region in said base region, electrically connected to a base electrode,

wherein said base contact section is constructed of a repeating structure in a plan view, in which a high impurity concentration region of the second conductivity type and a region of the second conductivity type constituting said base region arranged in an alternate manner from a side of said emitter region.

3. A semiconductor device according to claim 1 or 2, wherein said emitter region comprises a plurality of stripe regions and said base contact section comprises a plurality of contact sections formed along each of said plurality of stripe regions in said base region between said plurality of stripe regions.

4. A semiconductor device according to claim 1 or 2, wherein said base region comprises a plurality of regions exposed in a matrix pattern in said emitter region and said base contact section comprises a plurality of contact sections formed at each of a plurality of regions of said base region exposed in the matrix pattern.

5. A semiconductor device according to claim 3 or 4, wherein an emitter electrode connected to said emitter region and a base electrode connected to said base contact section are formed in respective comb structures in which teeth of said emitter electrode and said base electrode are engaged with each other being alternately arranged.

6. A semiconductor device according to claim 1 or 2, wherein said emitter region comprises a plurality of stripe regions and said stripe regions are formed so as to expose said base region at respective central portions of said stripe regions and an emitter electrode is formed, being connected to said stripe regions, so as to cover exposed portions of said base region via an insulating film.

7. A semiconductor device according to claim 6, wherein said base region exposed at the central portion of each of said stripe regions is segmented into a plurality along a direction of the stripe.

8. A semiconductor device according to claim 6, wherein said base region exposed at the central portion of each of said stripe regions is provided such that each of said stripe regions is segmented along a direction of the stripe and said emitter electrode is formed over the two segmented stripe regions and said base region exposed therebetween.

9. A semiconductor device with a bipolar transistor comprising:

a first conductivity type semiconductor layer serving as a collector region;

a base region constituted of a second conductivity type region provided in said first conductivity type semiconductor layer;

an emitter region constituted of a first conductivity region provided in said base region; and

a base contact section provided oppositely from said emitter region in said base region, electrically connected to a base electrode,

wherein said emitter region comprises a plurality of stripe regions and said stripe regions are formed so as to expose said base region at respective central portions of said stripe regions and an emitter electrode is formed, being connected to said stripe regions, so as to cover exposed portions of said base region.

10. A semiconductor device according to claim 9, wherein said base region exposed at the central portion of each of said stripe regions is segmented into a plurality along a direction of the stripe.

11. A semiconductor device according to claim 9, wherein said base region exposed at the central portion of each of said stripe regions is provided such that each of said stripe regions is segmented along a direction of the stripe and said emitter electrode is formed over the two segmented stripe regions and said base region exposed therebetween via an insulating film.

FIG.1

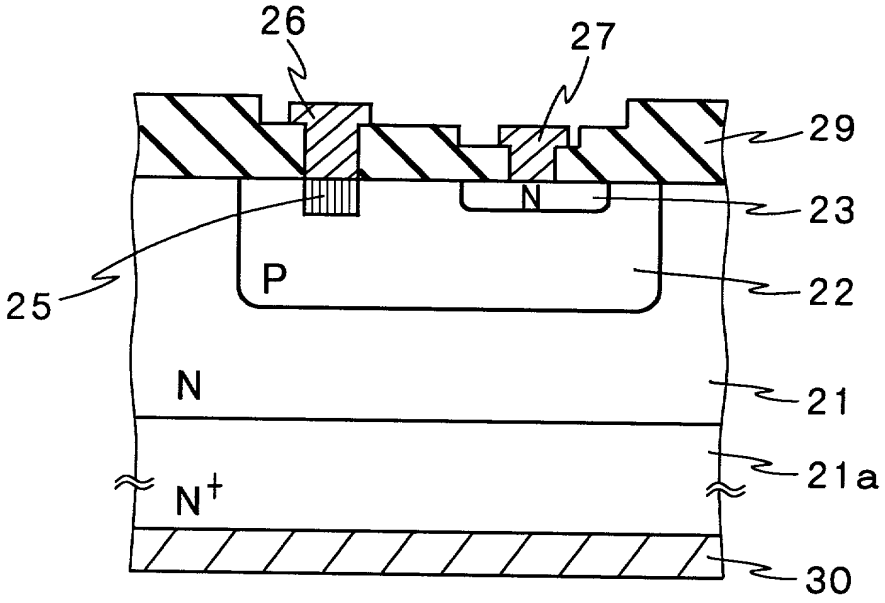

26
27
29
N
23
25
P
22
N
21
N+
21a
30

FIG.2

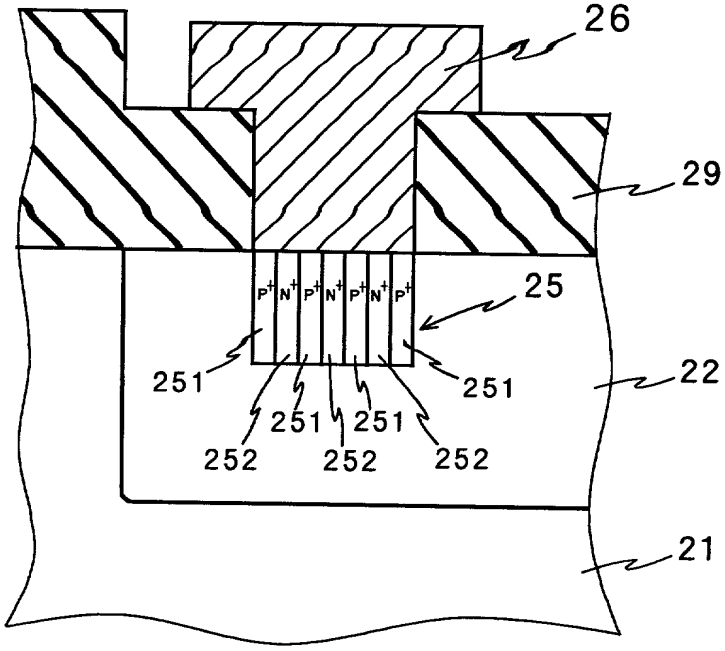

26
29
P+ N+ P+ N+ P+ N+ P+
25
251
251
22
251
251
252
252
252
21

FIG.3

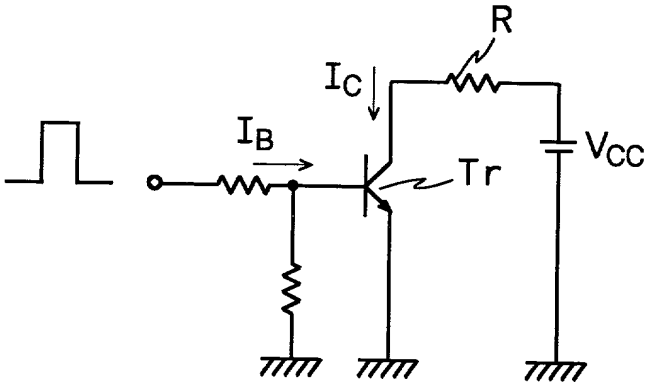


FIG.4 (a)

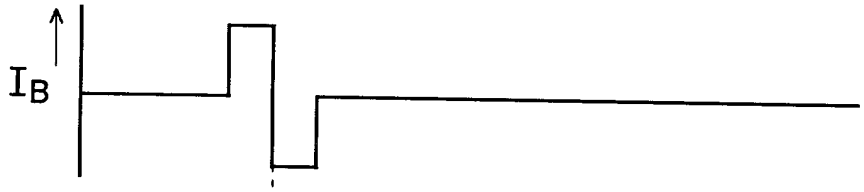


FIG.4 (b)

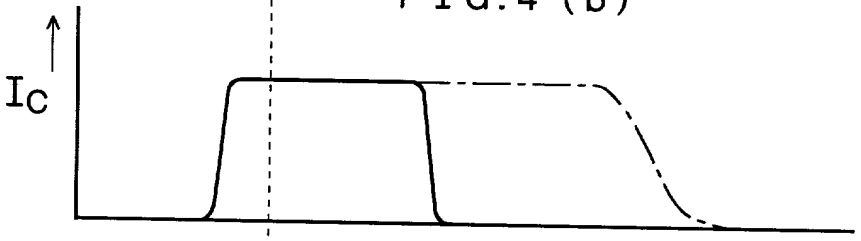
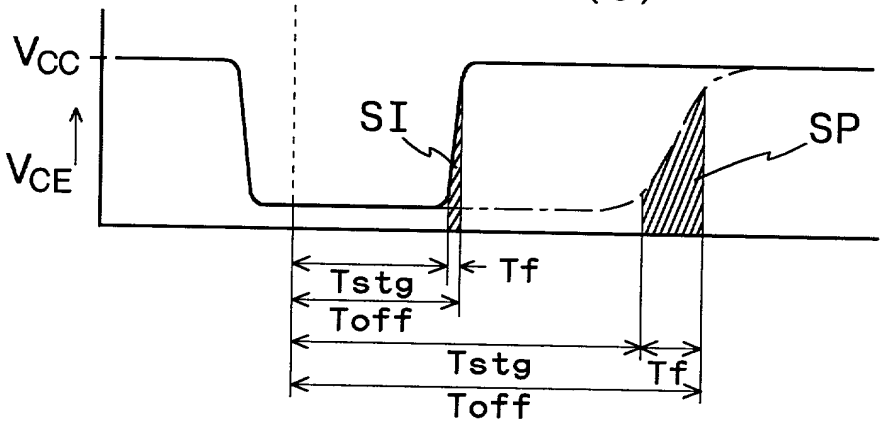


FIG.4 (c)



09/926425

FIG.5

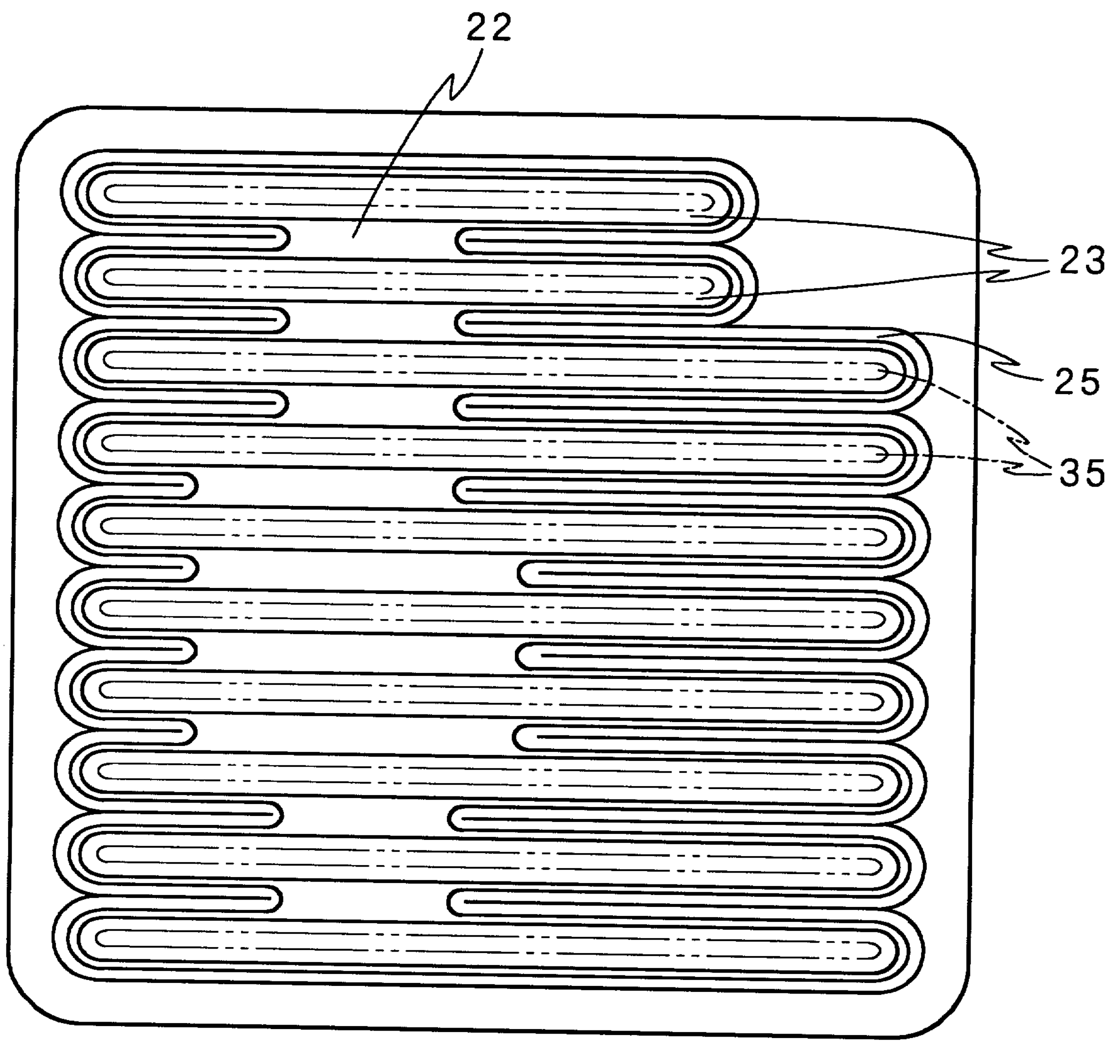


FIG.6

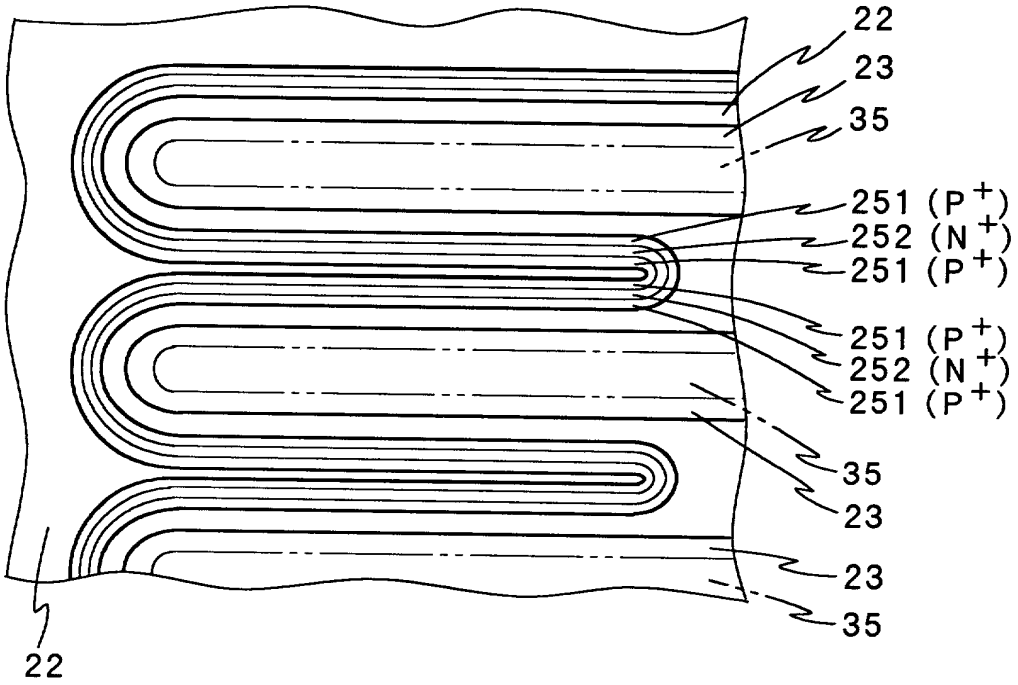


FIG.7

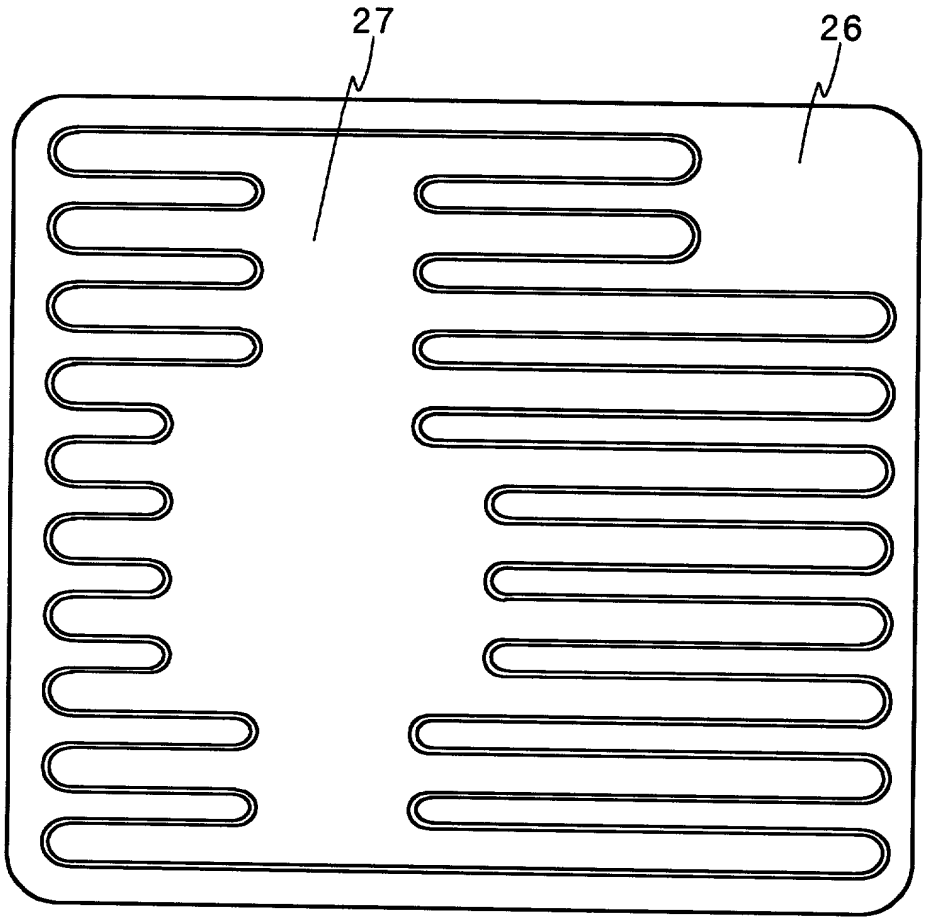


FIG.8

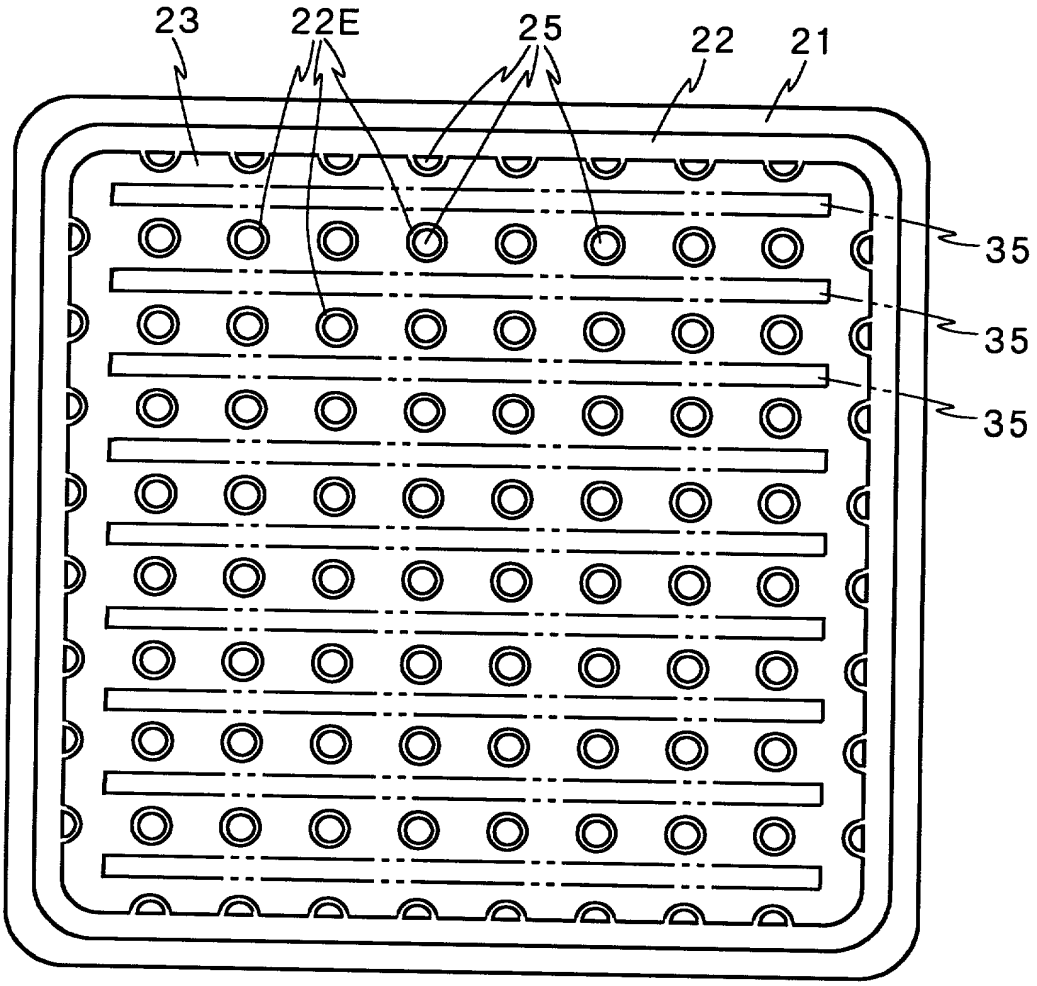


FIG.9

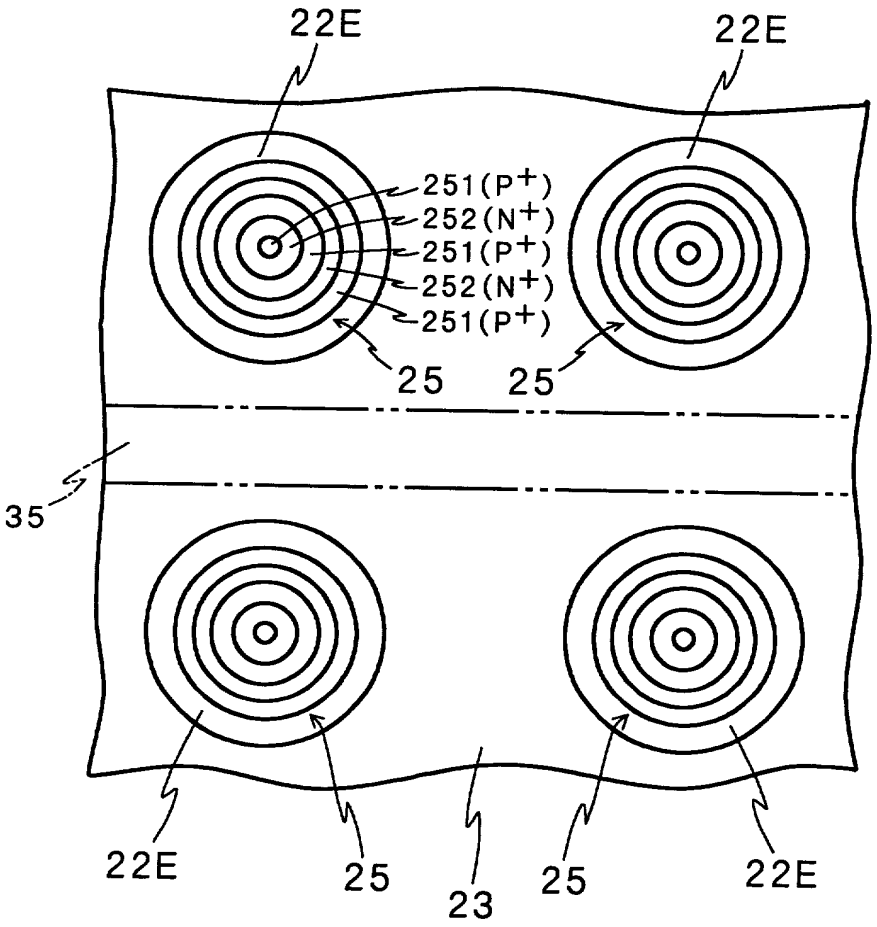


FIG.10

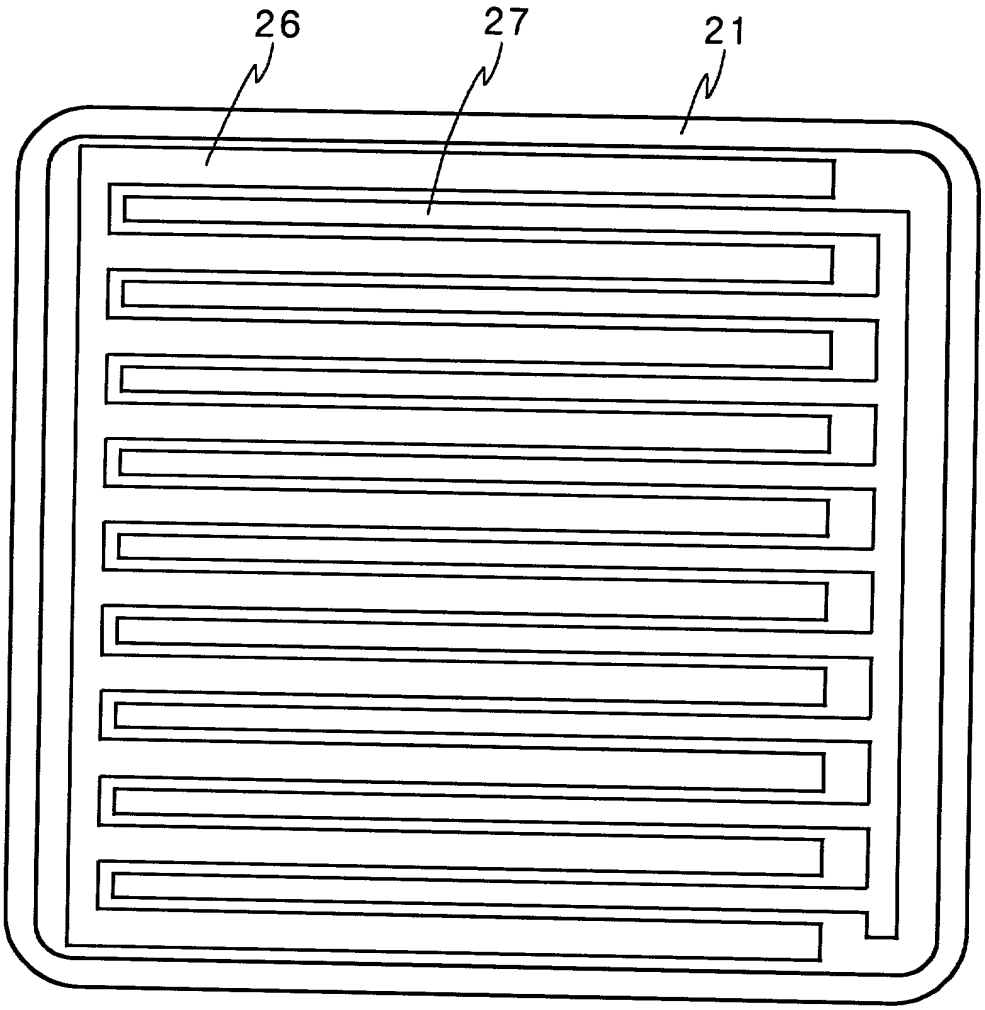


FIG.11

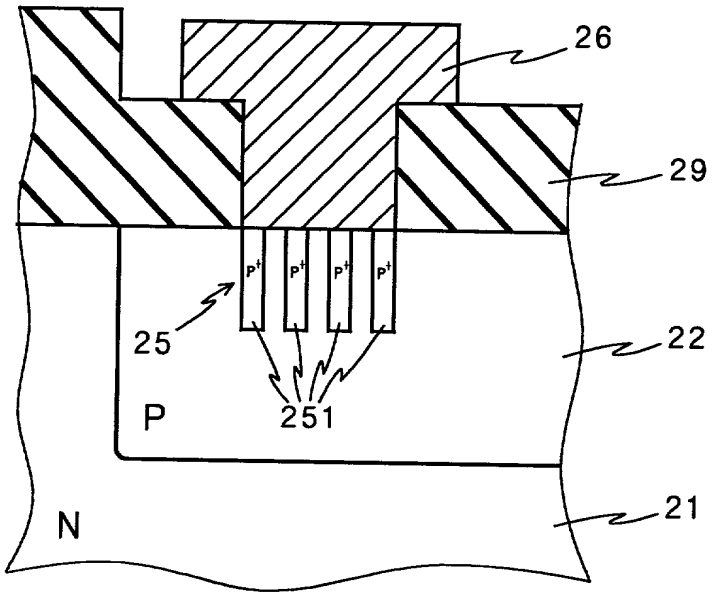

26
29
25
P+
22
P
251
N
21

FIG.12

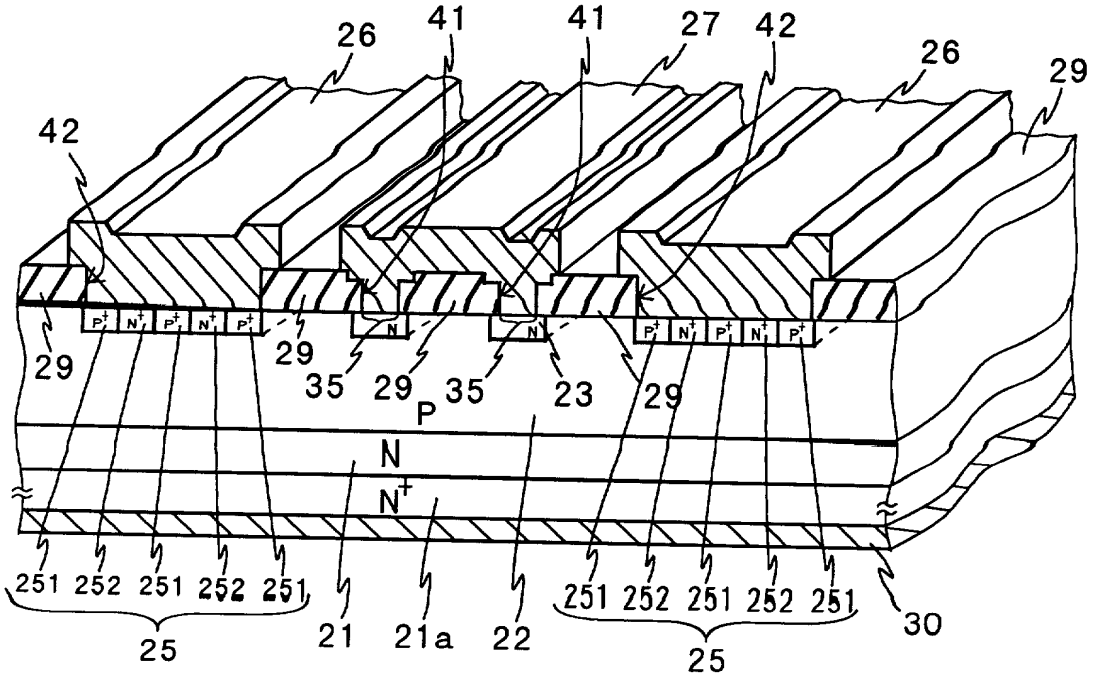

26
41
41
27
42
26
29
42
29
29
35
29
35
23
29
P
N
N+
251 252 251 252 251
25
21
21a
22
251 252 251 252 251
25
30

FIG.13

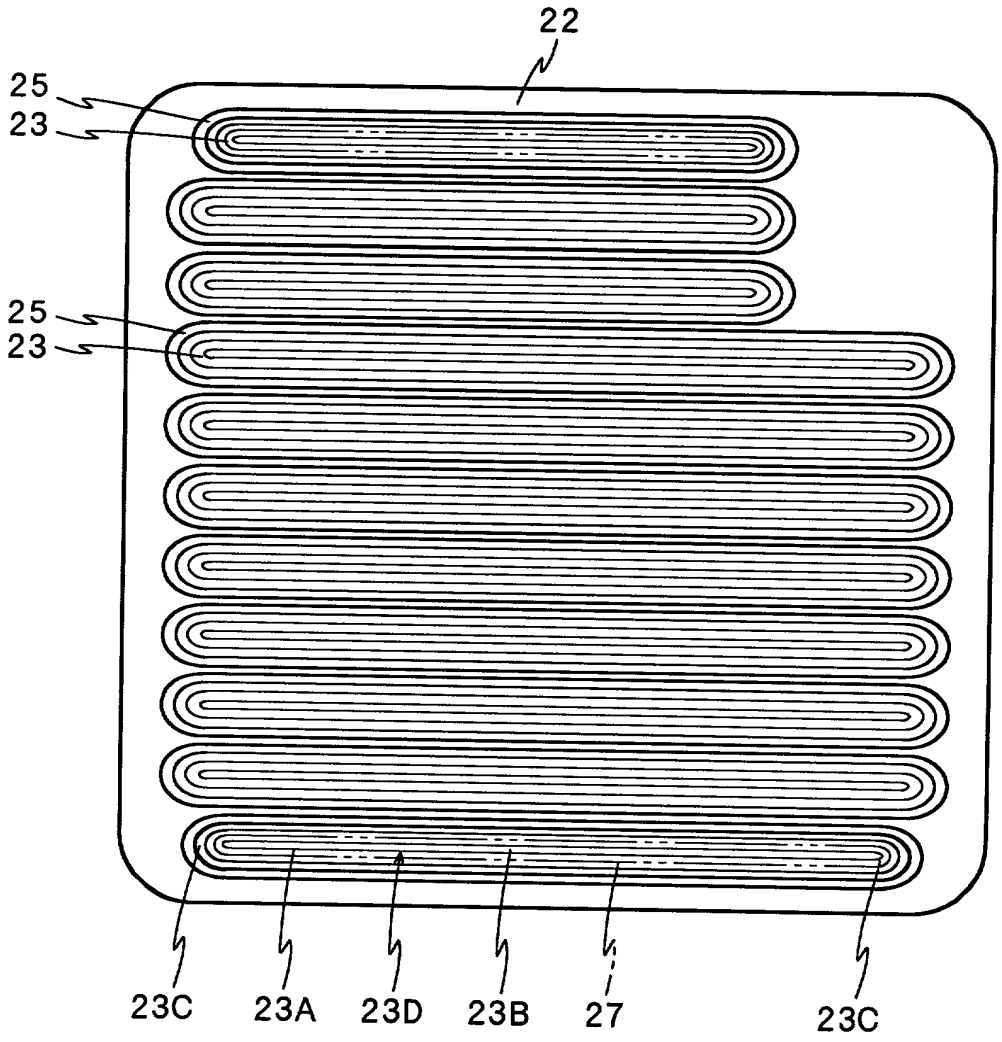


FIG.14

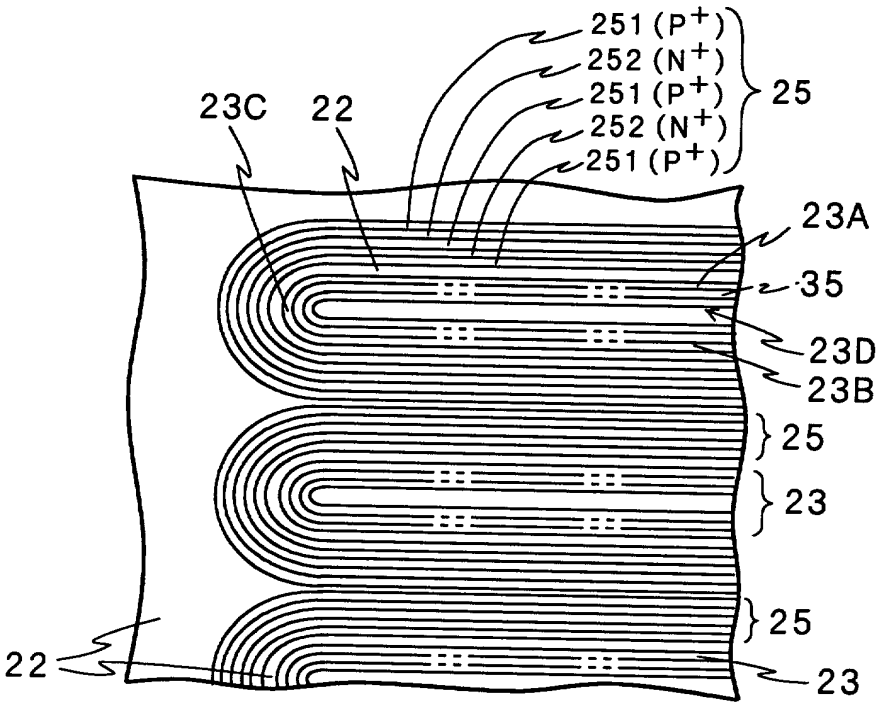


FIG.15

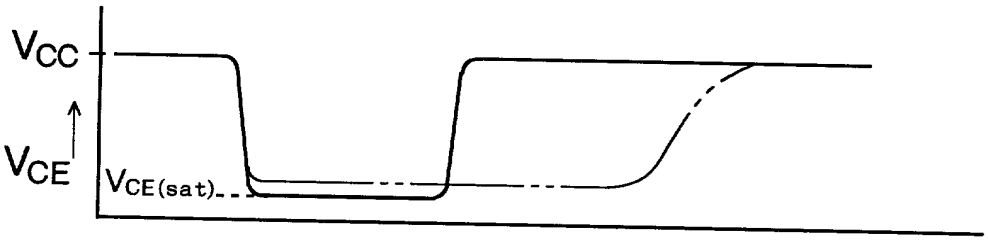


FIG.16

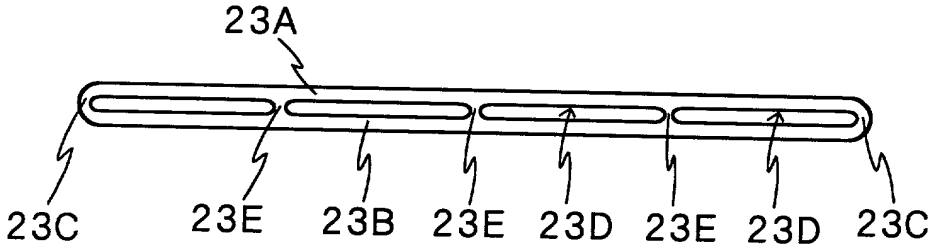


FIG.17

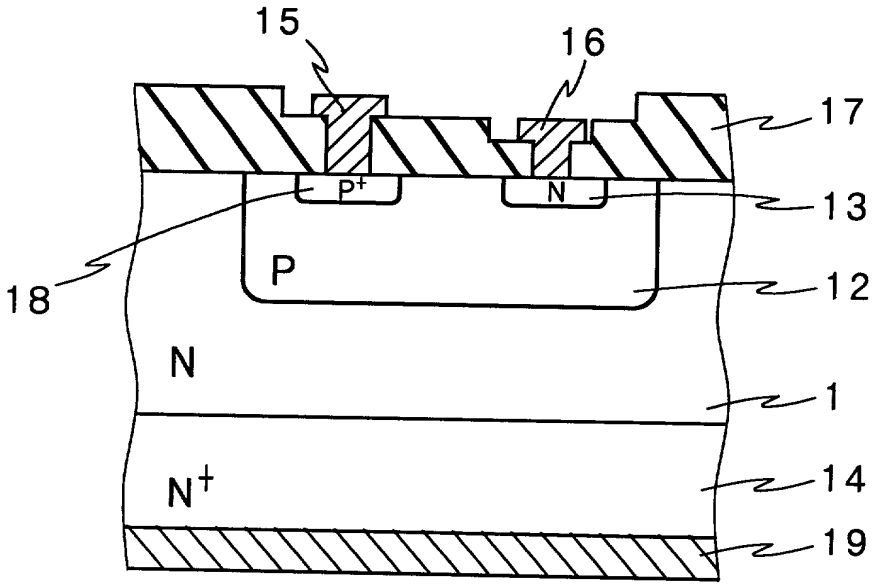


FIG.18

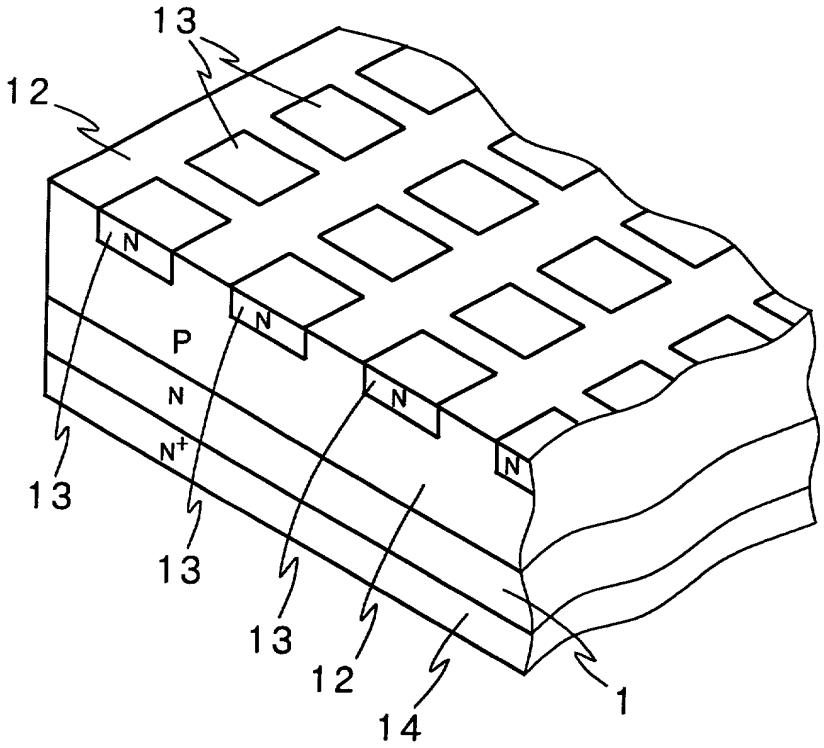


FIG.19

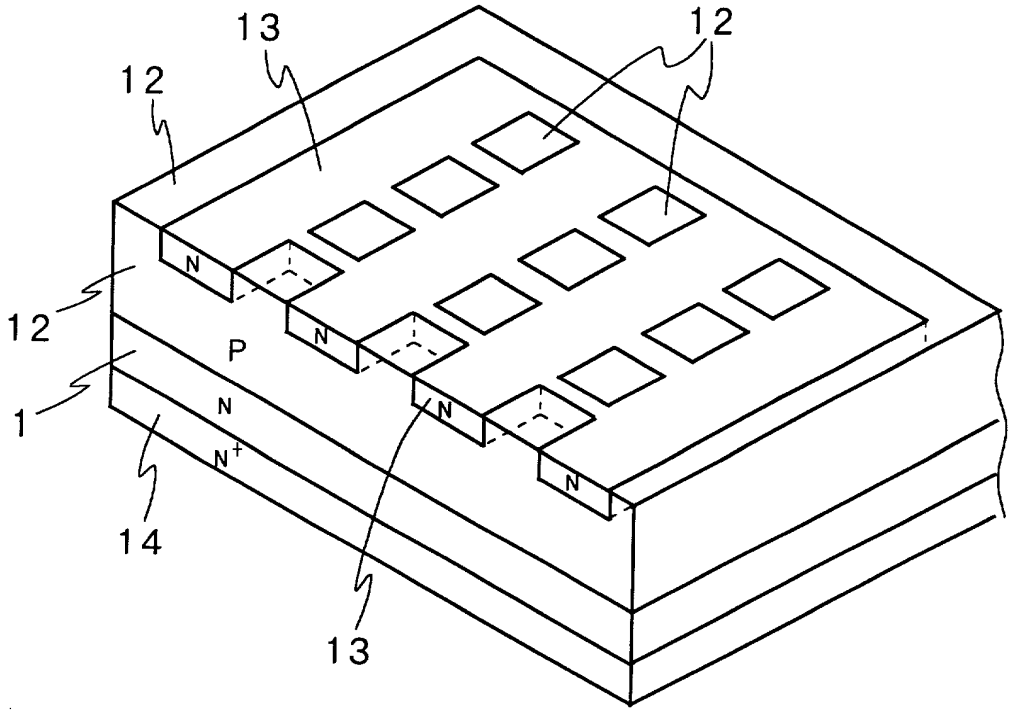
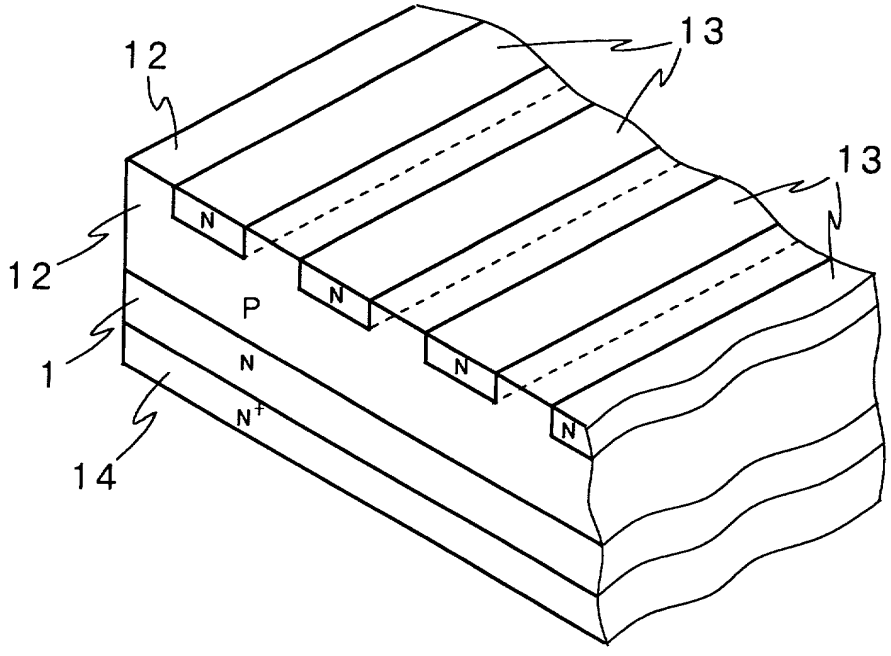


FIG.20



PTO/SB/10b (6-95)
Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE WITH BIPOLAR TRANSISTOR

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☒ was filed on April 28, 2000
as United States Application Number or
PCT International Application Number
PCT/JP00/02867 and was amended on
March 21, 2001 (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
H11-124515	Japan	30/04/1999	☐
H11-134477	Japan	14/05/1999	☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日及び国で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項に定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は発行許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

書類送付先

And I hereby appoint as principal attorneys: David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; George E. Oram, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; Martin S. Postman, Reg. No. 18,570; E. Marcie Emas, Reg. No. 32,131; Douglas H. Goldhush, Reg. No. 33,125; Kevin C. Brown, Reg. No. 32,402; Monica Chin Kitts, Reg. No. 36,105; Richard J. Berman, Reg. No. 39,107; King L. Wong, Reg. No. 37,500; Karen K. Costantino, Reg. No. 35,107; and James A. Poulos, III, Reg. No. 31,714.

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発明者の署名 日付	Inventor's signature Date Kazuhisa Sakamoto 19/10/2001
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第二共同発明者名	Full name of second joint inventor, if any
第二共同発明者の署名 日付	Second inventor's signature Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

第三共同発明者名		Full name of third joint inventor, if any	
第三共同発明者の署名	日付	Third inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第四共同発明者名		Full name of fourth joint inventor, if any	
第四共同発明者の署名	日付	Fourth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第五共同発明者名		Full name of fifth joint inventor, if any	
第五共同発明者の署名	日付	Fifth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第六共同発明者名		Full name of sixth joint inventor, if any	
第六共同発明者の署名	日付	Sixth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	

第七共同発明者名		Full name of seventh joint inventor, if any	
第七共同発明者の署名	日付	Seventh inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第八共同発明者名		Full name of eighth joint inventor, if any	
第八共同発明者の署名	日付	Eighth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第九共同発明者名		Full name of ninth joint inventor, if any	
第九共同発明者の署名	日付	Ninth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第十共同発明者名		Full name of tenth joint inventor, if any	
第十共同発明者の署名	日付	Tenth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	